Highly Linear Upconverter MMIC Designs with Complete Package and Test Board Effects for CDMA Applications

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Abstract — **1.9 GHz upconverter MMICs are designed and implemented using GaAs HBT foundry process. A crucial goal for the design is to achieve the high linearity required in CDMA systems with low idle currents. In addition, complete package and test board effects need to be considered rigorously. The proposed design adopts a class-AB input stage in a Gilbert cell to enhance the linearity. Another design based on the conventional emitter degeneration technique is also implemented on the same chip for comparison. The chip is finally housed in a 24-pin bump-chip carrier (BCC) package and surface-mounted on a test board. Both RF and LO ports are internally matched to 50 Ω on chip. A single supply voltage of 3V is used. The measured results show that with a reference input power of -10 dBm for IS-95 CDMA applications, the class-AB design achieves an adjacent channel power ratio (ACPR) of -44.9 dBc with a consumed current of 15 mA, while the emitter degeneration design achieves an ACPR of -43.8 dBc with a consumed current of 28.5 mA. Package and test board effects are analyzed using the 3-D EM simulation tool and transformed into the equivalent-circuit elements. The simulation including package and test board effects can predict the measured results quite well.**

I. INTRODUCTION

CDMA techniques are expanding rapidly in the 3rd generation mobile communications because they can increase channel capacity and data rate substantially, and meanwhile reduce the multi-path fading effects and power consumption effectively. However, these remarkable achievements are at the expense of high linearity requirement in an RF transceiver, especially in the transmitter. An upconverter that takes charges of frequency conversion in the transmitter is often required to have strictly low ACPR when applied to CDMA systems. As a matter of fact, the improvement of linearity using the conventional emitter-degeneration techniques is good but not efficient in power consumption. Many other techniques have been also reported to emphasize the pronounced enhancement in linearity. They are summarized to include the feedforward [1],[2], predistorter [3], shunt feedback [4], and class-AB input stage [5] techniques. It is difficult to be integrated into single chip for the first technique because of the complexity in architecture. For the second technique, an analog predistorter like a diode usually cannot compensate the upconverter nonlinearity satisfactorily. A digital one has much better performance but needs extra digital-signal-processing circuitry. With a feedback circuit, the third technique improves the linearity at the cost of poor isolation. In addition, it requires a larger chip area for layout of this feedback circuit that is usually composed of inductors and capacitors. A class-AB input stage design in the last technique can increase the consumed current with input power automatically to push the gain-compression point to a higher power level. This not only enhances the linearity but also lowers the idle current. Both features are the essential factors in designing CDMA transmitter circuits.

This paper compares the linearity-enhanced upconverters between two different design techniques, the class-AB input stage and emitter degeneration. Both circuits are implemented on the same chip using a GaAs HBT foundry process with f_T up to 30 GHz and housed in a single 24-pin BCC package. The interconnections of package and test board are considered carefully to evaluate their effects on the designed upconverters with the help of an EM simulation tool. It has been studied in our previous work that this kind of package may cause significant gain reduction under certain conditions [6].

II. DESIGN OF A CLASS-AB INPUT STAGE

To achieve a high linearity, the upconverter usually needs to make some concessions in gain, noise, current consumption, and chip size. An upconverter based on Gilbert mixer incorporating a class-AB input stage as shown in Fig. 1 can be used to improve linearity effectively without the above-mentioned expenses. The input stage contains the transistors, Q1, Q2, Q3 and Q4, in which Q2 acts as a current mirror of Q1. The input (IF) signal is applied to Q1 in common-emitter configuration and Q3 in common-base configuration simultaneously. The collector of Q1 is also connected to the emitter of Q3 such that both transistors switch in the opposite state when driven by the input signal. Q4 is used to balance the voltage drop due to Q3 for maintaining good differential

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properties in a Gilbert cell. In the positive cycle of input signal, Q1,Q2 and Q4 switch on while Q3 switches off. In the negative cycle, Q3 switches on instead but Q1,Q2 and Q4 are in the off state. This switching phenomenon can be observed from the simulated collector waveforms in Q3 and Q4, as shown in Fig. 2. Fig. 3 shows the simulated direct current components of collector currents versus the input signal voltage. It can be seen that the collector direct currents in Q3 and Q4, I_{C3} and I_{C4}, increase quite symmetrically with the amplitude of the input signal in negative and positive cycle respectively. Their output differential current, $I_C = I_{C3} - I_{C4}$, is almost linear with the input signal voltage and does not exhibit the compression phenomenon, no matter how large the amplitude of input signal will be. This explains why this technique can enhance the linearity so obviously. Actually, the linearity will be still limited due to the output differential voltage that has compression when the corresponding collector voltages, V_{C3} and V_{C4}, are clipped at higher amplitude of the input signal, as shown in Fig. 4.

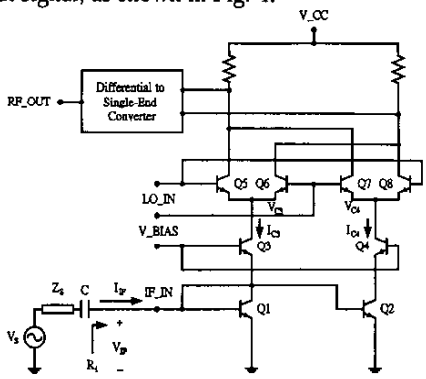

Fig. 1. Design of a class-AB input stage in a Gilbert cell of an upconverter.

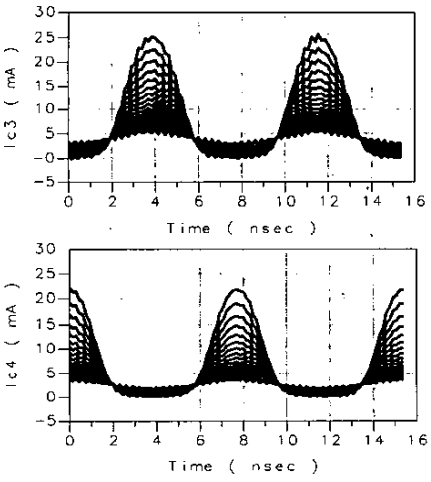

Fig. 2. Simulated collector current waveforms for the transistors Q3 and Q4 shown in Fig. 1.

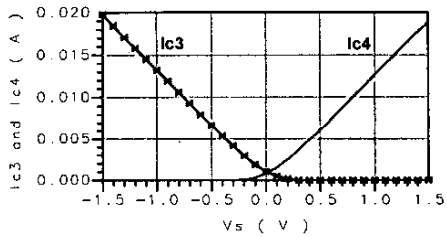

Fig. 3. Simulated direct current components of the collector currents in Q3 and Q4 versus the input signal voltage.

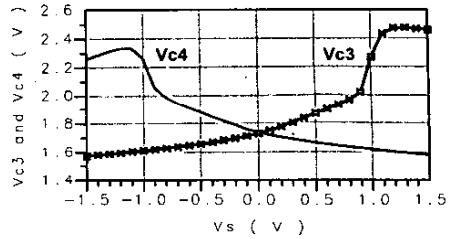

Fig. 4. Simulated direct current components of the collector voltages in Q3 and Q4 versus the input signal voltage.

The 3rd order intermodulation distortion (IMD_3) can be estimated as three times the third harmonic distortion (HD3) given in [5]. That is

$$IMD_3 \approx 3 \cdot HD3 \approx \frac{1}{16}\left(\frac{|I_{IF}|}{2 \cdot I_C}\right)^2 \quad (1)$$

where $|I_{IF}|$ represents the current amplitude of input IF signal. The relation between input resistance and collector current can be also approximated as

$$R_i \approx V_T / (2 \cdot I_C) \quad (2)$$

where V_T represents the thermal voltage. The input IF power is generally expressed as

$$P_{IF} = \frac{1}{2} |I_{IF}|^2 R_i . \quad (3)$$

After substituting (2) and (3) into (1), we can express IMD_3 in terms of P_{IF}, R_i, and V_T. That is

$$IMD_3 \approx \frac{1}{16} \frac{2 P_{IF} R_i}{V_T^2} . \quad (4)$$

For a two-tone input, assume that each tone has a power of -13 dBm and the total power for two tones is equal to -10 dBm. The corresponding collector current is about 15 mA from the simulation. The thermal voltage is approximately 0.026 V at room temperature, T=300°K. The calculated quantity of R_i using (2) is 0.87 Ω. With these quantities, the calculated IMD_3 using (4) is equal to 8.1×10^{-3} or -41.8 dBc. The input third-order intercept point (IIP_3) can be further evaluated using the formula

$$IIP_3\,(\text{dBm}) = P_{IF}\,(\text{dBm}) - \frac{1}{2} IMD3\,(\text{dBc}) . \quad (5)$$

The calculated quantity of IIP_3 is equal to 7.9 dBm.

III. Evaluation of Package and Test Board Effects

Generally speaking, the manufactured integrated circuits need to be packaged for convenient use on test board. In this work, the designed chip has been packaged with a 24-pin BCC package and then surface-mounted on a test board. Since the GaAs substrate is semi-insulated, the interconnections realized on chip have negligible parasitic effects when compared to those in package and test board. In the package, the bondwires that connect between the pads on chip and the pins of package act as series inductances. On the test board, the signal traces in microstrip forms have parasitic elements including series inductances and shunt capacitances for themselves, and mutual inductances and capacitances from one to the other. A series resistance and a shunt conductance can be used to represent the trace loss and substrate loss, respectively. In Fig. 5, we show the equivalent parasitic elements for those package and test-board interconnections that have significant effects on RF signal transmission and grounding. Fig. 6 shows an example of the 3-D configuration of part of the package and test-board interconnections in PakSi-E, a commercially available EM simulation tool, for evaluating their equivalent parasitic-element quantities. The complete calculated results for the parasitic elements shown in Fig. 5 are listed in Table I.

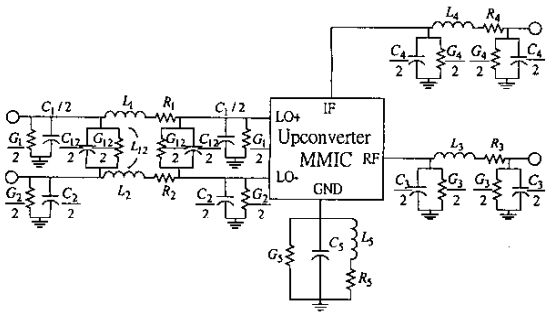

Fig. 5. The equivalent parasitic elements of package and test-board interconnections that are considered in the simulation.

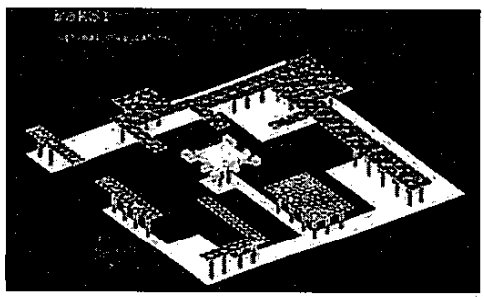

Fig. 6. The 3-D configuration of package and test-board interconnections shown in PakSi-E for evaluating their equivalent ground parasitic elements.

TABLE I
EQUIVALENT PARASITIC-ELEMENT QUANTITIES

Net n	L_n (nH)	R_n (mΩ)	C_n (pF)	G_n (μS)
LO + (n=1)	3.565e+0	5.465e+1	5.965e-1	1.241e+0
LO – (n=2)	2.319e+0	4.342e+1	4.541e-1	1.387e+0
RF (n=3)	4.160e+0	4.603e+1	1.080e+0	3.036e+0
IF (n=4)	6.634e+0	5.687e+1	1.319e+0	4.586e+0
GND (n=5)	1.334e-1	4.575e+0	4.417e-1	1.104e+0
Mutual Term		**L_{12} (nH)**	**C_{12} (pF)**	**G_{12} (μS)**
LO + & LO – (n=1&2)		2.922e-1	1.032e-1	4.406e-1

IV. Results and Discussion

The chip that was finally fabricated includes two upconverter designs. One has adopted a class-AB input stage in the Gilbert mixer for linearity enhancement while the other uses the emitter-degeneration circuit instead. In each deign, a differential to single-ended converter has been included to convert the differential RF signal at the mixer output to a single-ended signal for the convenience of measurement. It is noted that both RF and LO ports are internally matched to 50 Ω on chip. The chip with an area of 1.5 mm × 1.0 mm was housed in a 24-pin BCC package with an overall dimension of 4 mm × 4 mm × 0.8 mm. Finally, the packaged chip was surface-mounted on a test board with an area of 20 mm × 20 mm, as shown in Fig. 7.

The IF, LO and RF frequencies used in the upconverters are 130 MHz, 1750MHz and 1880MHz, respectively. A single supply voltage of 3V is used. The applied LO power is –3 dBm. For the design with a class-AB input stage, the crucial parameters under the CW test include a conversion gain (G_C) equal to –6.7 dB and an output third-order intermodulation distortion (IMD_3) equal to –43.5 dBc with respect to a –13 dBm two-tone input. It is noted that this measured IMD_3 is close to our theoretically predicted value, -41.8 dBc. The slight discrepancy is due to an overestimation of R_i in (2). By referring to [5], the input resistance, R_i, decreases with a larger amplitude of the input signal, which will further reduce IMD_3 by a couple of dB according to (4). When the IS-95 CDMA signal with respect to –10 dBm power is applied to the input, the measured ACPR is –44.9 dBc. The consumed current in measurement of the above parameters is about 15 mA, which also agrees with our original prediction.

The measured results including G_C, IMD_3, ACPR, and the consumed current for the upconverter design using emitter degeneration under the same test conditions are –1.67 dB, -38.5 dBc, -43.8 dBc, and 28.5 mA, respectively. From the comparison, one can know that the former

design is superior to the latter in consuming less direct current but maintaining almost the same ACPR. However, the former design has the disadvantage of lower conversion gain. More detailed comparisons of the measured parameters between two different designs can be seen in Figs. 8-10.

In Fig. 8 we can see that the simulated conversion gains versus input IF power agree quite well with measurements. The package and test board effects cause a conversion-gain reduction about 3 dB for both cases. These gain reductions are primarily due to the loss and impedance mismatch in the bondwires and PCB traces that are connected to RF, LO, and IF terminals, and also the imperfect grounding, in the designed MMICs.

V. Conclusions

In this paper, a highly linear upconverter design incorporating a class-AB input stage has been demonstrated to achieve much lower direct current consumption than the conventional design using emitter degeneration without scarifying the ACPR performance in a CDMA system. This paper also shows estimation of the complete package and test board effects with the help of a 3-D EM simulation tool for evaluation of the corresponding parasitic-element quantities. The agreement between simulation and measurement is quite satisfactory.

VI. Acknowledgments

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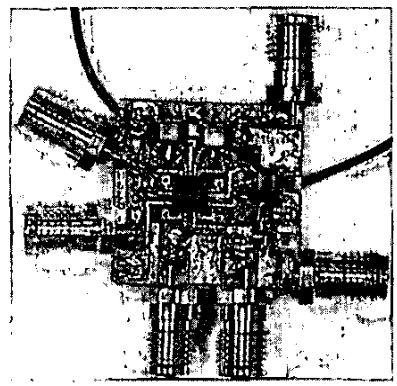

Fig. 7. Photo of the packaged chip on the test board.

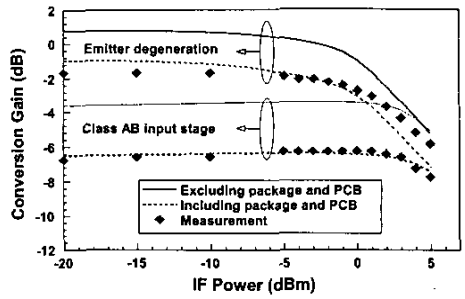

Fig. 8. Comparison of the simulated conversion gains between two different upconverter designs with measurements.

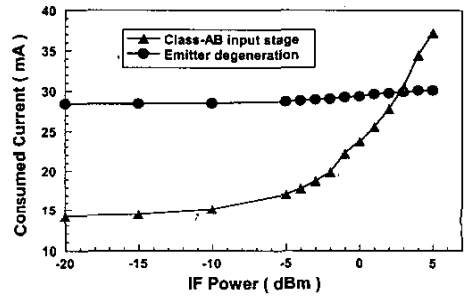

Fig. 9. Comparison of the measured consumed currents between two different upconverter designs.

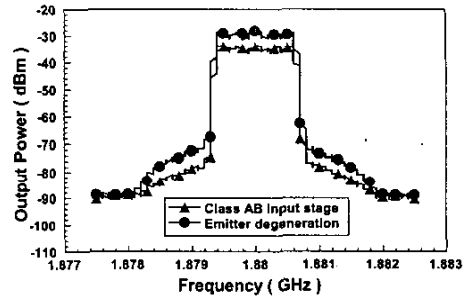

Fig. 10. Comparison of the measured output spectra between two different upconverter designs at the input power of -10 dBm.